Green-Mode PWM Controller with High-Voltage Start-Up Circuit and Adjustable OLP Delay Time

REV. 03

General Description

The LD7576X series bring high performance, combines with highly integrated functions, protections and EMI-improve solution. It's an ideal solution for those cost-sensitive system, reducing component count and overall system cost.

The LD7576X series features near-lossless high voltage startup circuit, green-mode power-saving operation, leading-edge blanking of the current sensing and internal slope compensation. They also consist with more protections of OLP (Over Load Protection), OVP (Over Voltage Protection) and OTP (Over Temperature Protection) to prevent the circuit damage under abnormal conditions.

The LD7576X series are available in DIP-8 and SOP-8 package.

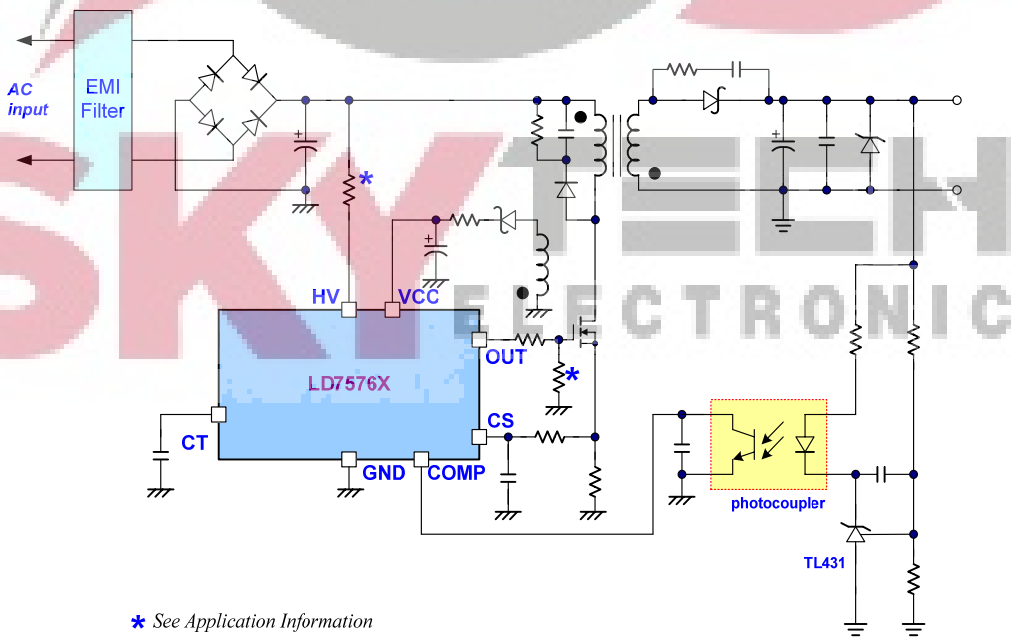
Features

- High-Voltage (500V) Startup Circuit
- Current Mode Control
- Non-Audible-Noise Green Mode Control
- UVLO (Under Voltage Lockout)
- LEB (Leading-Edge Blanking) on CS Pin
- Internal Slope Compensation
- OVP (Over Voltage Protection) on Vcc
- On-Chip OTP (Over Temperature Protection)
- OLP (Over Load Protection)
- Latch Mode Protection by CT pin
- 500mA Driving Capability
- Adjustable OLP delay time

Applications

- Switching AC/DC Adaptor and Battery Charger
- Open Frame Switching Power Supply
- LCD Monitor/TV Power

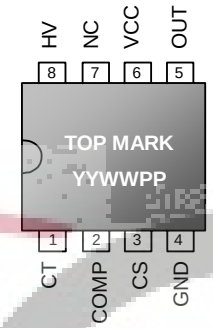
Typical Application



* *See Application Information*

Pin Configuration

SOP-8 & DIP-8 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Protection/Frequency	Package		Top Mark	Shipping
LD7576 PS	Auto-Recovery/65KHz	SOP-8	PB Free	LD7576PS	2500 /tape & reel
LD7576 GS	Auto-Recovery/65KHz	SOP-8	Green Package	LD7576GS	2500 /tape & reel
LD7576 PN	Auto-Recovery65KHz	DIP-8	PB Free	LD7576PN	3600 /tube /Carton
LD7576J PS	Auto-Recovery/100KHz	SOP-8	PB Free	LD7576JPS	2500 /tape & reel
LD7576J GS	Auto-Recovery/100KHz	SOP-8	Green Package	LD7576JGS	2500 /tape & reel
LD7576J PN	Auto-Recovery100KHz	DIP-8	PB Free	LD7576JPN	3600 /tube /Carton
LD7576H PS	Latch/65KHz	SOP-8	PB Free	LD7576HPS	2500 /tape & reel
LD7576H GS	Latch/65KHz	SOP-8	Green Package	LD7576HGS	2500 /tape & reel
LD7576H PN	Latch/65KHz	DIP-8	PB Free	LD7576HPN	3600 /tube /Carton
LD7576K PS	Latch/100KHz	SOP-8	PB Free	LD7576KPS	2500 /tape & reel
LD7576K GS	Latch/100KHz	SOP-8	Green Package	LD7576KGS	2500 /tape & reel
LD7576K PN	Latch/100KHz	DIP-8	PB Free	LD7576KPN	3600 /tube /Carton

The LD7576 is ROHS compliant/ Green Package.

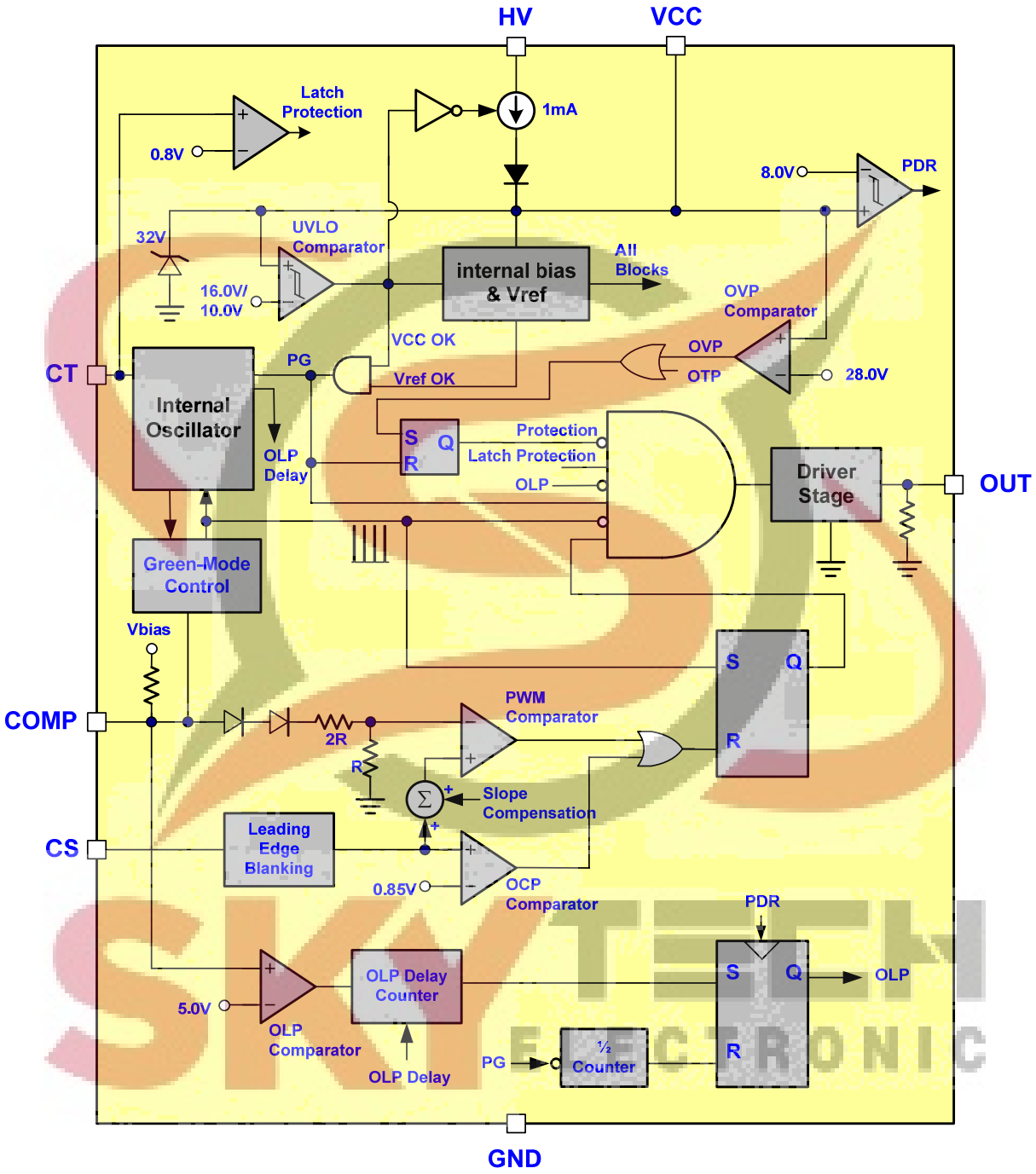
Note:

1. Oscillating frequency:
   LD7576/76H: 65KHz (typ.),
   LD7576J/76K: 100KHz (typ.).
2. LD7576H/76K features Built-in latch-mode function of OVP on Vcc pin , OLP and On Chip OTP.
3. LD7576/76J features Built-in Auto-Recovery function of OVP on Vcc pin OLP and On Chip OTP.

Pin Descriptions

PIN	NAME	FUNCTION
1	CT	This pin is to program the frequency of the low frequency timer. By connecting a capacitor to ground to set the OLP delay time. And this pin can be used for latch mode protection. By pulling this pin lower than 0.8 V, the controller will be entered latch mode until the AC power-on recycling.
2	COMP	Voltage feedback pin (same as the COMP pin in UC384X), By connecting a photo-coupler to close the control loop and achieve the regulation. A high quality ceramic capacitor (X7R) is required for general applications (102pF at least).
3	CS	Current sense pin, connect to sense the MOSFET current
4	GND	Ground
5	OUT	Gate drive output to drive the external MOSFET
6	VCC	Supply voltage pin
7	NC	Unconnected Pin
8	HV	Connect this pin to positive terminal of bulk capacitor to provide the startup current for the controller. When Vcc voltage trips the UVLO(on), this HV loop will be off to save the power loss on the startup circuit.

Block Diagram



Absolute Maximum Ratings

Supply Voltage VCC	30V
High-Voltage Pin, HV	-0.3V~600V
COMP, CT, CS	-0.3 ~7V
Junction Temperature	150°C
Operating Ambient Temperature	-40°C to 85°C
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8)	160°C/W
Package Thermal Resistance (DIP-8)	100°C/W
Power Dissipation (SOP-8, at Ambient Temperature = 85°C)	400mW
Power Dissipation (DIP-8, at Ambient Temperature = 85°C)	650mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (except HV Pin)	3KV
ESD Voltage Protection, Machine Model	300V
Gate Output Current	500mA

Caution:

Stresses beyond the ratings specified in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Supply Voltage V_{CC}	11	25	V
V_{CC} Capacitor	10	47	μF
CT Value	0.047	0.1	μF
COMP Pin Capacitor	1	100	nF

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
High-Voltage Supply (HV Pin)					
High-Voltage Current Source	Vcc< UVLO(on),HV=500V	0.5	1.0	1.5	mA
Off-State Leakage Current	Vcc> UVLO(off),HV=500V			35	μA
Supply Voltage (VCC Pin)					
Startup Current				100	μA
Operating Current (with 1nF load on OUT pin)	V_{COMP}=0V		2.7	3.5	mA
	V_{COMP}=3V		3.1	4.0	mA
	OLP tripped		0.5		mA
	OVP tripped		0.6		mA
	OTP tripped		0.5		mA
	Latch Protection		2.0		mA
UVLO (off)		9.0	10.0	11.0	V
UVLO (on)		15.0	16.0	17.0	V
OVP Level		26.5	28.0	29.5	V
Voltage Feedback (COMP Pin)					
Short Circuit Current	V_{COMP}=0V		1.3	2.2	mA
Open Loop Voltage	COMP pin open		5.6		V
Green Mode Threshold VCOMP			2.35		V
Current Sensing (CS Pin)					
Maximum Input Voltage		0.80	0.85	0.90	V
Leading Edge Blanking Time			230		nS
Input impedance		1			MΩ
Delay to Output			100		nS
Oscillator for Switching Frequency					
Frequency	LD7576/76H	61.0	65.0	69.0	KHz
	LD7576J/76K	94.0	100.0	106.0	KHz
Green Mode Frequency	LD7576/76H		20		KHz
	LD7576J/76K		32		KHz
Trembling Frequency	LD7576/76H		± 4.0		KHz
	LD7576J/76K		± 6.0		KHz
Temp. Stability	(-40°C ~105°C)			5	%
Voltage Stability	(VCC=11V-25V)			1	%

Electrical Characteristics

(T_A = +25°C unless otherwise stated, V_{CC}=15.0V)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Low Frequency Timer (CT Pin)					
Low Frequency Period	CT=0.047μF		4.7		mS
Temp. Stability	(-40°C ~105°C)			5	%
Voltage Stability	(VCC=11V-25V)			1	%
Gate Drive Output (OUT Pin)					
Output Low Level	VCC=15V, Io=20mA			1	V
Output High Level	VCC=15V, Io=20mA	8			V
Rising Time	Load Capacitance=1000pF		50	160	nS
Falling Time	Load Capacitance=1000pF		30	60	nS
OLP (Over Load Protection)					
OLP Trip Level			5.0		V
OLP Delay Time	CT=0.1μF		110		mS
	CT=0.047μF		45		mS
OTP (Over Temperature)					
OTP Level			140		°C
OTP Hysteresis			30		°C
Latch Protection					
CT Pin Trip Level for Latch Protection	Low Activated			0.8	V
Timer for Power-on Verification			250		mS
De-Latch Vcc Level		7.2	8	8.8	V

Typical Performance Characteristics

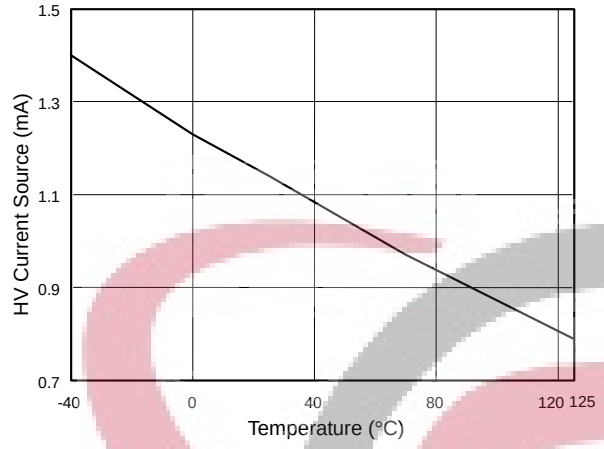


Fig. 1 HV Current Source vs. Temperature (HV=500V, Vcc=0V)

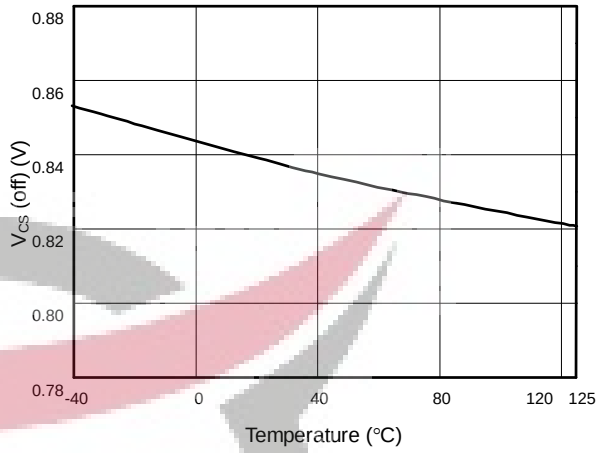


Fig. 2 V_{CS} (off) vs. Temperature

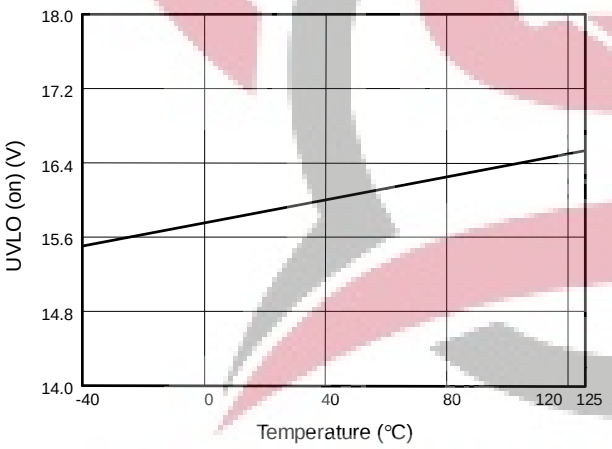


Fig. 3 UVLO (on) vs. Temperature

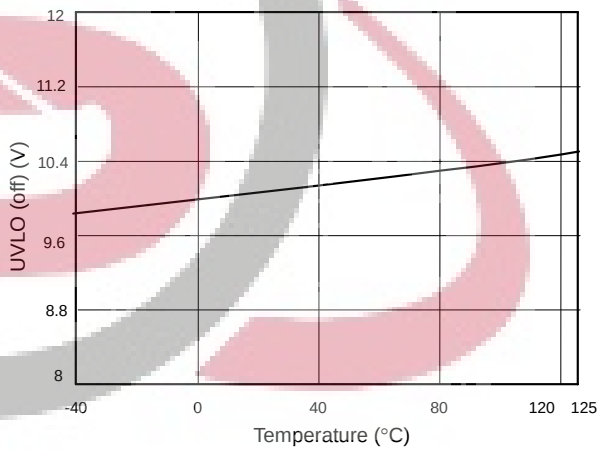


Fig. 4 UVLO (off) vs. Temperature

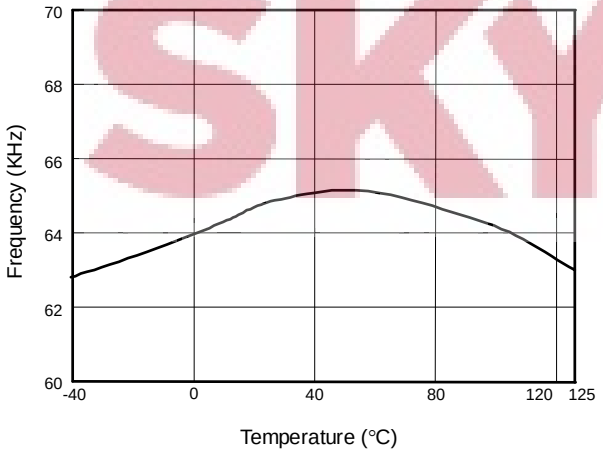


Fig. 5 Frequency vs. Temperature

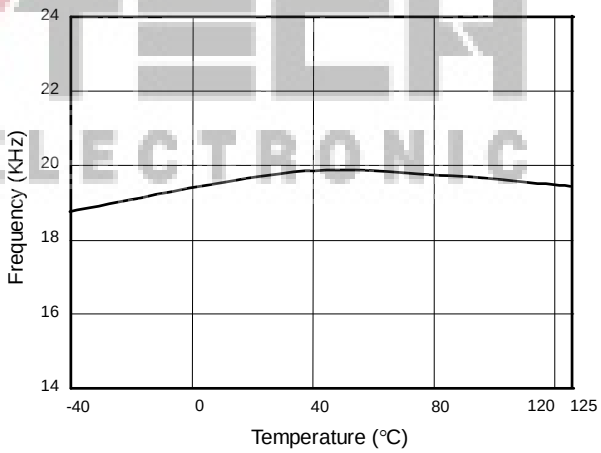


Fig. 6 Green Mode Frequency vs. Temperature

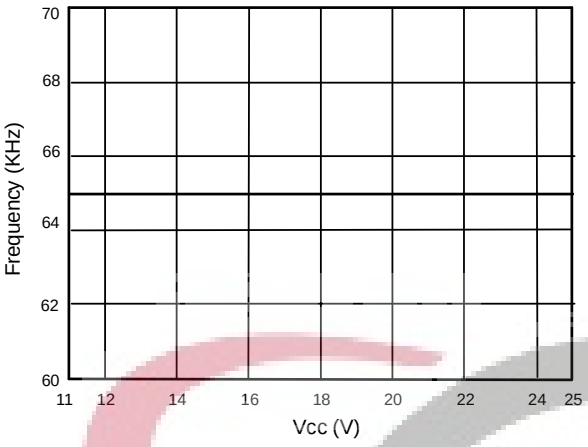


Fig. 7 Frequency vs. Vcc

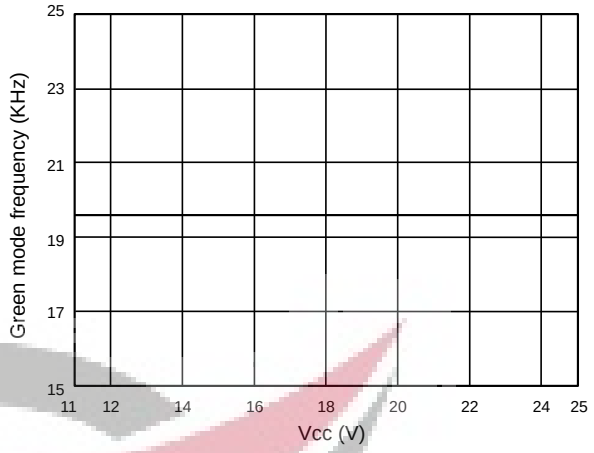


Fig. 8 Green mode frequency vs. Vcc

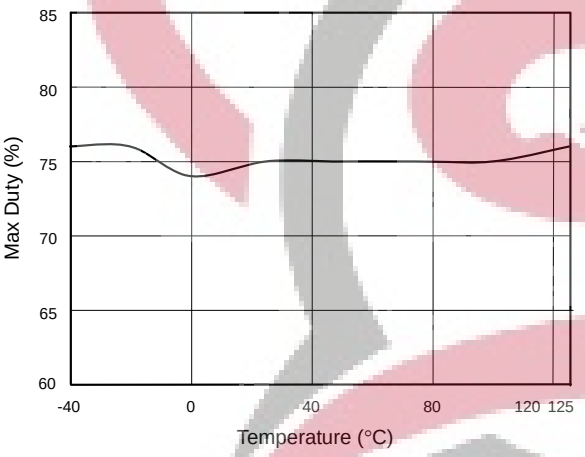


Fig. 9 Max Duty vs. Temperature

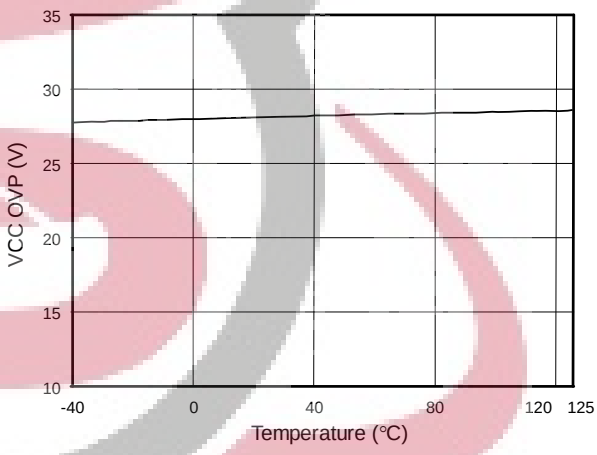


Fig. 10 VCC OVP vs. Temperature

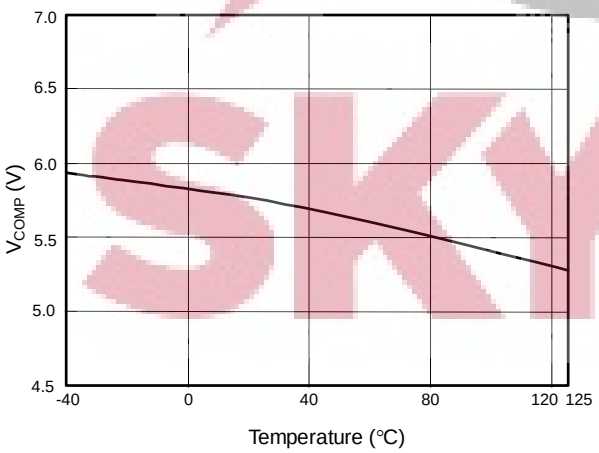


Fig. 11 V_{COMP} open loop voltage vs. Temperature

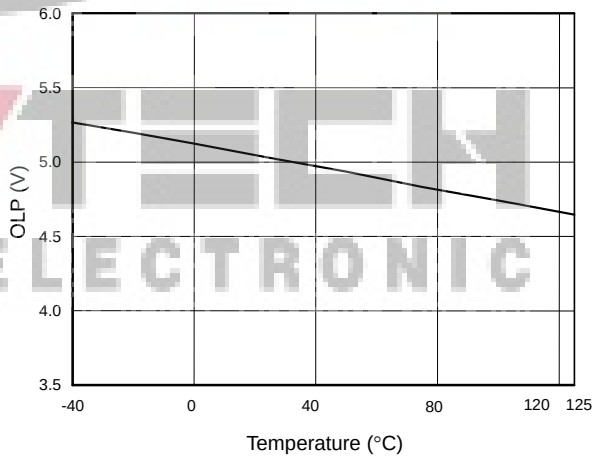


Fig. 12 OLP-Trip Level vs. Temperature

Application Information

Operation Overview

As long as the green power requirement becomes a trend and the power saving is getting more and more important for the switching power supplies and switching adaptors, the traditional PWM controllers are not able to support such new requirements. Furthermore, the cost and size limitation force the PWM controllers need to be powerful to integrate more functions to reduce the external part counts. The LD7576X series are ideal for these applications to provide an easy and cost effective solution; its detailed features are described as below.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

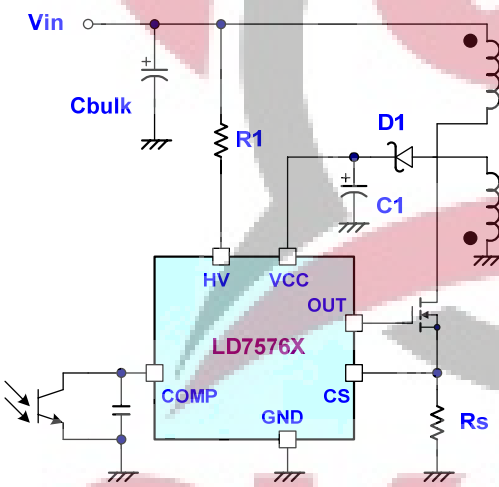


Fig. 13

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes too significant power to meet the current power saving requirement. In most cases, startup resistors carry large resistance. And larger resistance takes longer startup time.

To achieve the optimized topology, as shown in figure 13, LD7576X series are implemented with a high-voltage startup circuit for such requirement. During the startup, a high-voltage current source sinks current from the bulk capacitor to provide the startup current as well as charge the Vcc capacitor C1. During the startup transient, the Vcc drops lower than the UVLO threshold so the current source will be enabled to supply 1mA current. Meanwhile, the Vcc supply current is as low as 100μA that most of the HV current is adopted to charge the Vcc capacitor. By using such configuration, the turn-on delay time will be almost same no matter under low-line or high-line conditions.

As the Vcc voltage rises higher than UVLO(on) to power on the LD7576X series and further to deliver the gate drive signal, the high-voltage current source will be disabled and the supply current is provided from the auxiliary winding of the transformer. Therefore, it would eliminate the power loss on the startup circuit and perform highly power saving.

An UVLO comparator is embedded to detect the voltage on the Vcc pin to ensure the supply voltage enough to power on the LD7576X series PWM controller and in addition to drive the power MOSFET. As shown in Fig. 14, a hysteresis is provided to prevent the shutdown from the voltage dip during startup. The turn-on and turn-off threshold level are set at 16V and 10.0V, respectively.

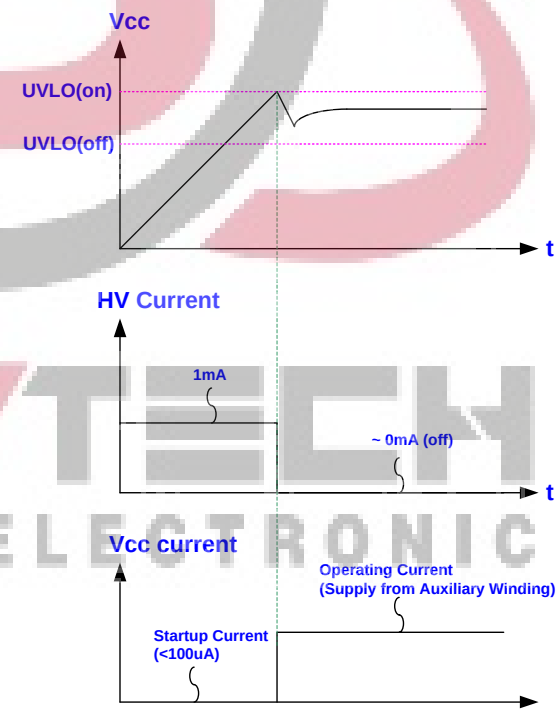


Fig. 14

Current Sensing, Leading-Edge Blanking and the Negative Spike on CS Pin

The typical current mode PWM controller feedbacks both current signal and voltage signal to close the control loop

and achieve regulation. The LD7576X series detects the primary MOSFET current from the CS pin, which is not only for the peak current mode control but also for the pulse-by-pulse current limit. The maximum voltage threshold of the current sensing pin is set at 0.85V. Thus the MOSFET peak current can be calculated as:

$$I_{PEAK(MAX)} = \frac{0.85V}{R_S}$$

A 230nS leading-edge blanking (LEB) time is provided in the input of CS pin to prevent false-triggering from the current spike. In the low power applications, if the total pulse width of the turn-on spikes is less than 230nS and the negative spike on the CS pin does not exceed -0.3V, the R-C filter (as shown in figure15) can be eliminated.

However, the total pulse width of the turn-on spike is related to the output power, circuit design and PCB layout. It is strongly recommended to add a small R-C filter (as shown in figure 16) for higher power application to avoid the CS pin from being damaged by the negative turn-on spike.

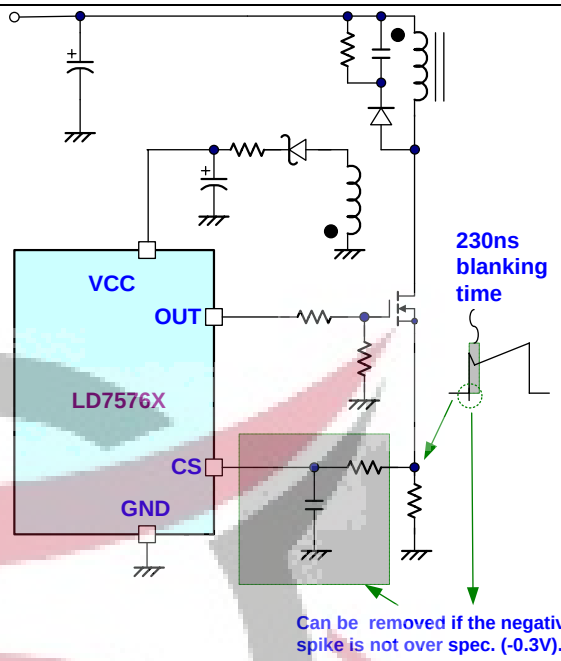


Fig. 15

Output Stage and Maximum Duty-Cycle

An output stage of a CMOS buffer, with typical 500mA driving capability, is incorporated to drive a power MOSFET directly. And the maximum duty-cycle of LD7576X series are limited to 75% to avoid the transformer saturation.

Voltage Feedback Loop

The voltage feedback signal is provided from the TL431 on the secondary side through the photo-coupler to the COMP pin of LD7576X series. The input stage of LD7576X series, like the UC384X, is with 2 diodes voltage offset to feed the voltage divider with 1/3 ratio, that is,

$$V_{+(PWM_{COMPARATOR})} = \frac{1}{3} \times (V_{COMP} - 2V_F)$$

A pull-high resistor is embedded internally to optimize the external circuit. Generally, an external capacitor in parallel to photo-coupler is required in application.

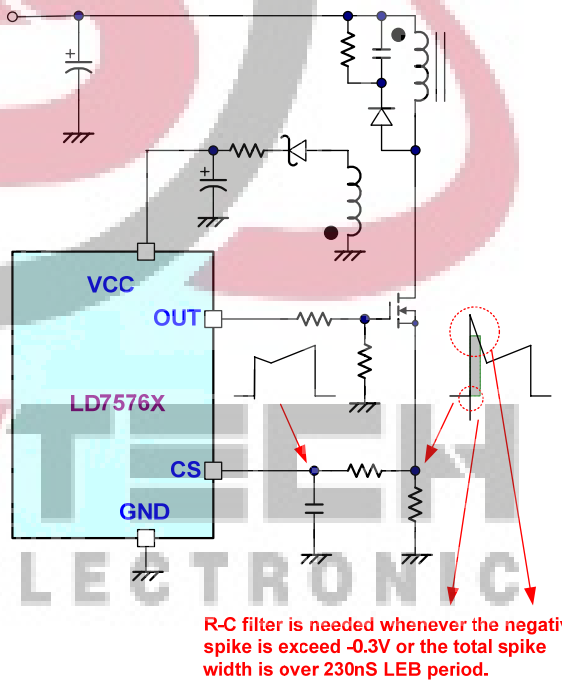


Fig. 16

Oscillator and Switching Frequency

The switching frequency of LD7576X series are fixed at 65KHz and 100KHz internally to provide the optimized

operations in consideration of the EMI performance, thermal treatment, component sizes and transformer design.

Internal Slope Compensation

A fundamental issue of current mode control is the stability problem when its duty-cycle is operated for more than 50%. To stabilize the control loop, the slope compensation is needed in the traditional UC384X design by injecting the ramp signal from the RT/CT pin through a coupling capacitor. In LD7576X series, the internal slope compensation circuit has been implemented to simplify the external circuit design.

On/Off Control

By pulling COMP pin lower than 1.2V will disable the gate output pin of LD7576X series immediately. The off mode can be released when the pull-low signal is removed.

Dual-Oscillator Green-Mode Operation

There are many different topologies has been implemented in different chips for the green-mode or power saving requirements such as “burst-mode control”, “skipping-cycle mode”, “variable off-time control “…etc. The basic operation theory of all these approaches intended to reduce the switching cycles under light-load or no-load condition either by skipping some switching pulses or reduce the switching frequency.

By using LD proprietary dual-oscillator technique, the green-mode frequency can be well controlled and further to avoid the generation of audible noise.

Over Load Protection (OLP) - Auto Recovery

To protect the circuit from being damaged during over load condition and short or open loop condition, the LD7576X series were implemented with smart OLP function. LD7576/76J features auto recovery function of it, see figure 17 for the waveform. In the example of the fault condition, the feedback system will force the voltage loop toward the saturation and then pull the voltage high on COMP pin (VCOMP). When the V_{COMP} ramps up to the OLP threshold of 5V and stays for longer than the OLP delay time, the protection will be activate and then turn off the gate output to stop the switching of power circuit. The OLP delay time, set by CT pin, is to prevent the false triggering from the power-on and turn-off transient. Higher CT value will generate longer OLP delay time. The recommended CT value will be 0.1μF when OLP delay time is for around 110mS and 0.047μF for around 55mS.

A divide-2 counter is implemented to reduce the average power under OLP behavior. Whenever OLP is activated, the output is latched off and the divide-2 counter starts to count the number of UVLO(off). The latch will be released when the 2nd UVLO(off) point started to counted then the output is recovered to switching again.

With the protection mechanism, the average input power will be minimized, so that the component temperature and stress can be controlled within the safe operating area.

Over Load Protection (OLP) - Latch mode

Other than LD7576/76J, the LD7576H/76K features latch mode of smart OLP protection. Figure 18 shows the waveform under fault condition. The feedback system will force the voltage loop toward the saturation and thus pull the voltage high on COMP pin (VCOMP). When the VCOMP ramps up to the OLP threshold of 5.0V and stays for longer than OLP delay time, the protection will be activated and then latch off the gate output to stop switching of the power circuit. The delay time is to prevent the false-triggering from power-on, turn-off transient and peak load condition. As soon as the over load condition is removed, the controller will be kept latched until the Vcc drops lower than 8V. It is necessary to start another AC power-on recycling to get the output back.

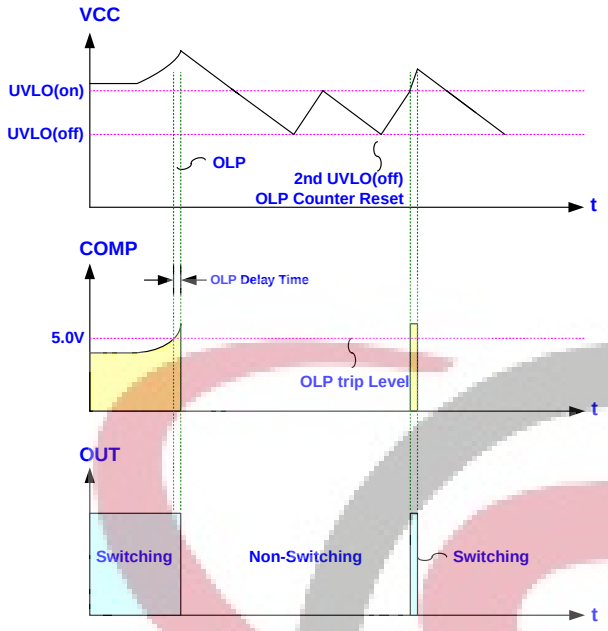


Fig. 17

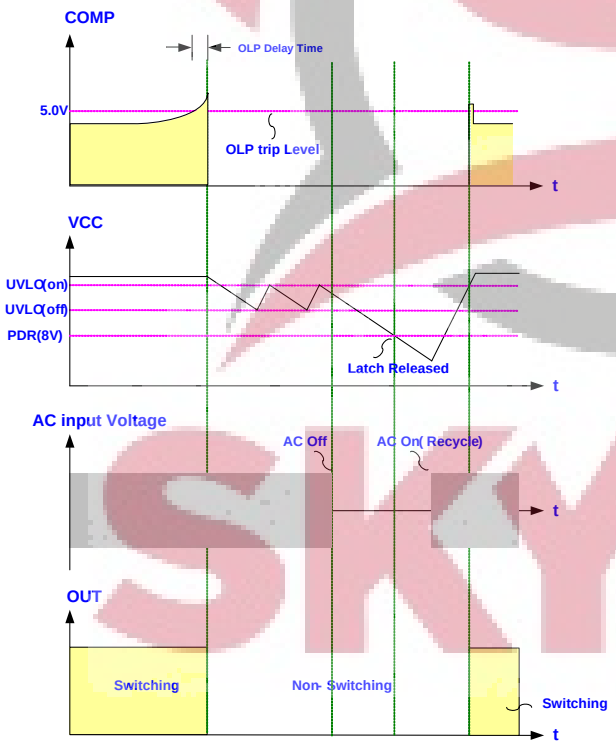


Fig. 18

OVP (Over Voltage Protection) on Vcc - Auto Recovery

The maximum V_{GS} ratings of the power MOSFETs are mostly for 30V. To prevent the V_{GS} enter fault condition, LD7576X series are implemented with OVP function on Vcc. Whenever the Vcc voltage is higher than the OVP threshold, the output gate drive circuit will be shutdown simultaneously and the switching of the power MOSFET is disabled until the next UVLO(on).

The Vcc OVP functions of LD7576/76J are auto-recoverable. If the OVP condition, usually caused by open-loop of feedback, is not released, the Vcc will tripped the OVP level again and re-shutdown the output. The Vcc works in hiccup mode. Figure 19 shows its operation.

Otherwise, when the OVP condition is removed, the Vcc level will be resumed and the output will automatically return to the normal operation.

OVP (Over Voltage Protection) on Vcc - Latch mode

As similar behavior like OLP latch-mode, whenever the voltage on the Vcc pin is higher than the OVP threshold, the output gate drive circuit will be shutdown simultaneous to latch off the switching of the power MOSFET. As soon as the voltage on Vcc pin drops below OVP threshold and starts AC-recycling again, it will recover to normal operation. Figure 20 shows its operation.

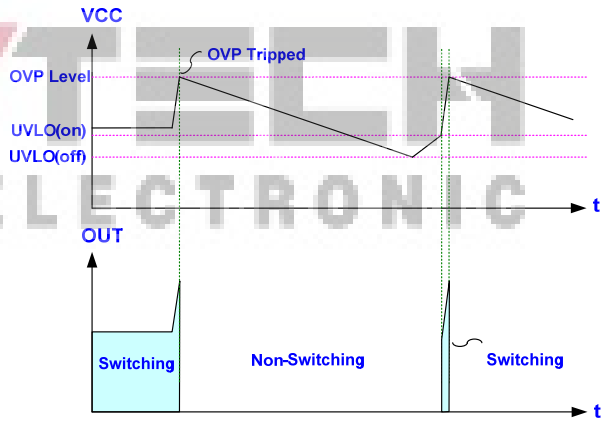


Fig. 19

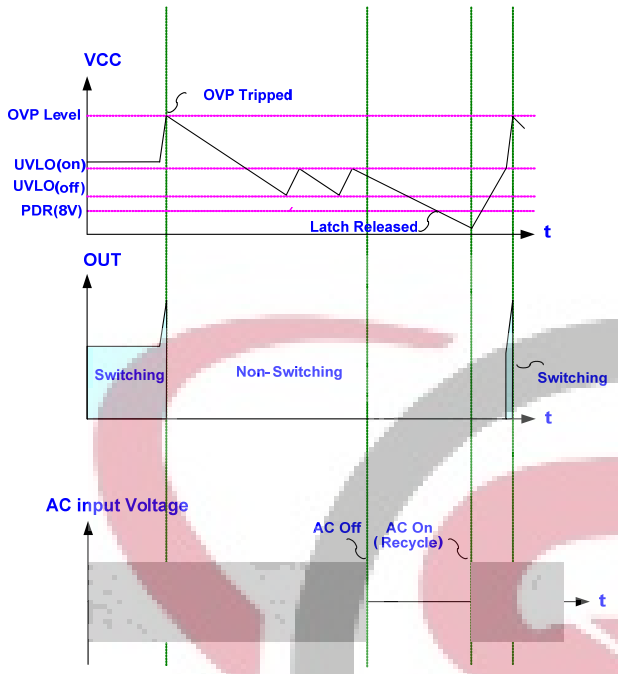


Fig. 20

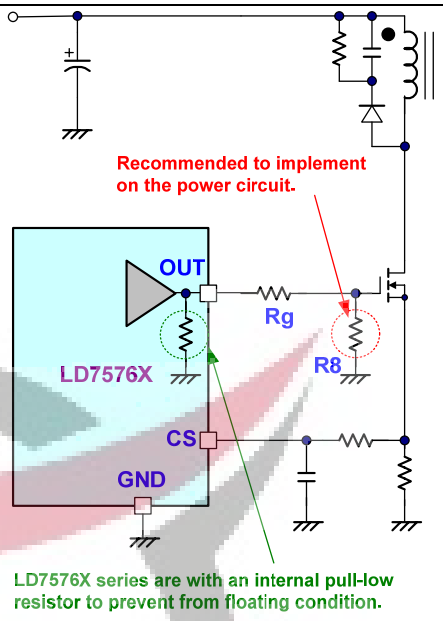


Fig. 21

Pull-Low Resistor on the Gate Pin of MOSFET

The LD7576X series consist with an anti-floating resistor on the OUT pin to protect the output from abnormally operation or false triggering of MOSFET. Even so, we still recommend adding an external one on the MOSFET gate terminal to provide more protection in case of disconnection of gate resistor R_G during power-on.

In such single-fault condition, as show in figure 22, the resistor R8 can provide a discharge path to avoid the MOSFET from being false-triggered by the current through the gate-to-drain capacitor C_{GD}. Therefore, the MOSFET is always pulled low and placed in the off-state whenever the gate resistor is disconnected or opened in any case.

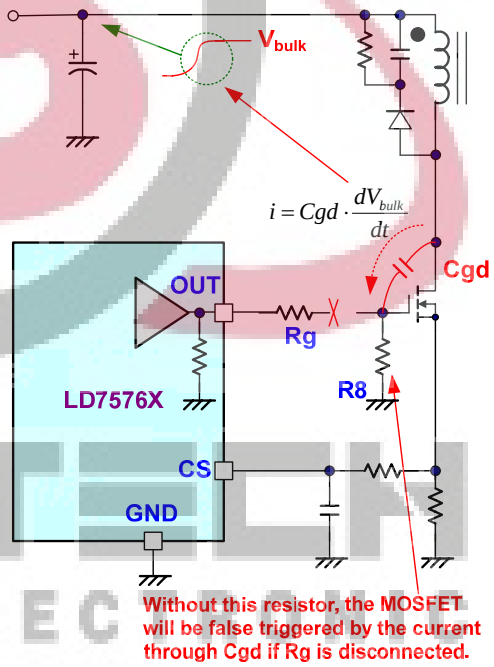


Fig. 22

Protection Resistor on the Hi-V Path

In some other Hi-V process and design, there may be a parasitic SCR caused around HV pin, Vcc and GND. As shown in figure 23, a small negative spike on the HV pin may trigger this parasitic SCR and cause latchup between Vcc and GND. It will intend to damage the chip because of the equivalent short-circuit induced by such latchup behavior.

Leadtrend's proprietary of Hi-V technology will eliminate parasitic SCR in LD7576X series. Figure 24 shows the equivalent circuit of LD7576X series of Hi-V structure. So that LD7576X series are more capable to sustain negative voltage than similar products. However, a 10KΩ resistor is recommended to be added on the Hi-V path to play as a current limit resistor whenever a negative voltage is applied.

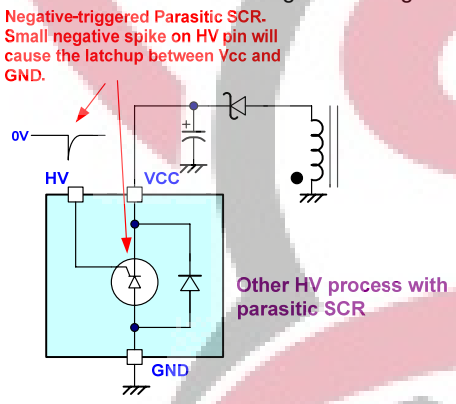


Fig. 23

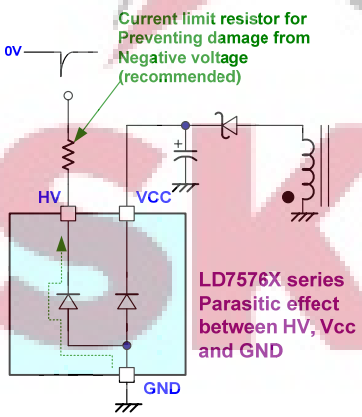


Fig. 24

On-Chip OTP

An internal OTP circuit is embedded inside the LD7576/76J to provide the worst-case protection for this controller. When the chip temperature rises higher than the trip OTP level, the output will be disabled until the chip is cooled down below the hysteresis window.

On-Chip OTP – Latch - Mode

As similar behavior like OLP and OVP on Vcc latch-mode, an internal OTP circuit are embedded with the LD7576H/76K to provide the worst-case protection for this controller. When the chip temperature rises higher than the trip OTP level, it shutdowns the output gate drive circuit simultaneously to latch off the switching of the power MOSFET. It won't recover unless the chip is cooled down below the OTP threshold and recycle again.

Latch-Mode Protection

The latch-mode protection in LD7576 series will be enabled by pulling the CT pin voltage below 0.8V. Figure 26 shows the operation. When the latch-mode is tripped, LD7576 series will shutdown the gate output and then latch-off the power supply. Unless the controllers re-plug and re-start to drop VCC below 8V, the gate output mode will remain latched. The detailed operation is depicted as figure 26.

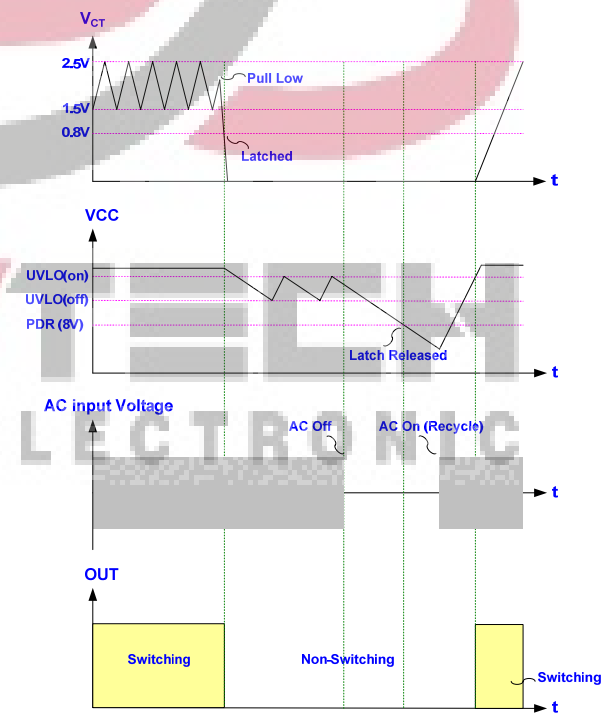
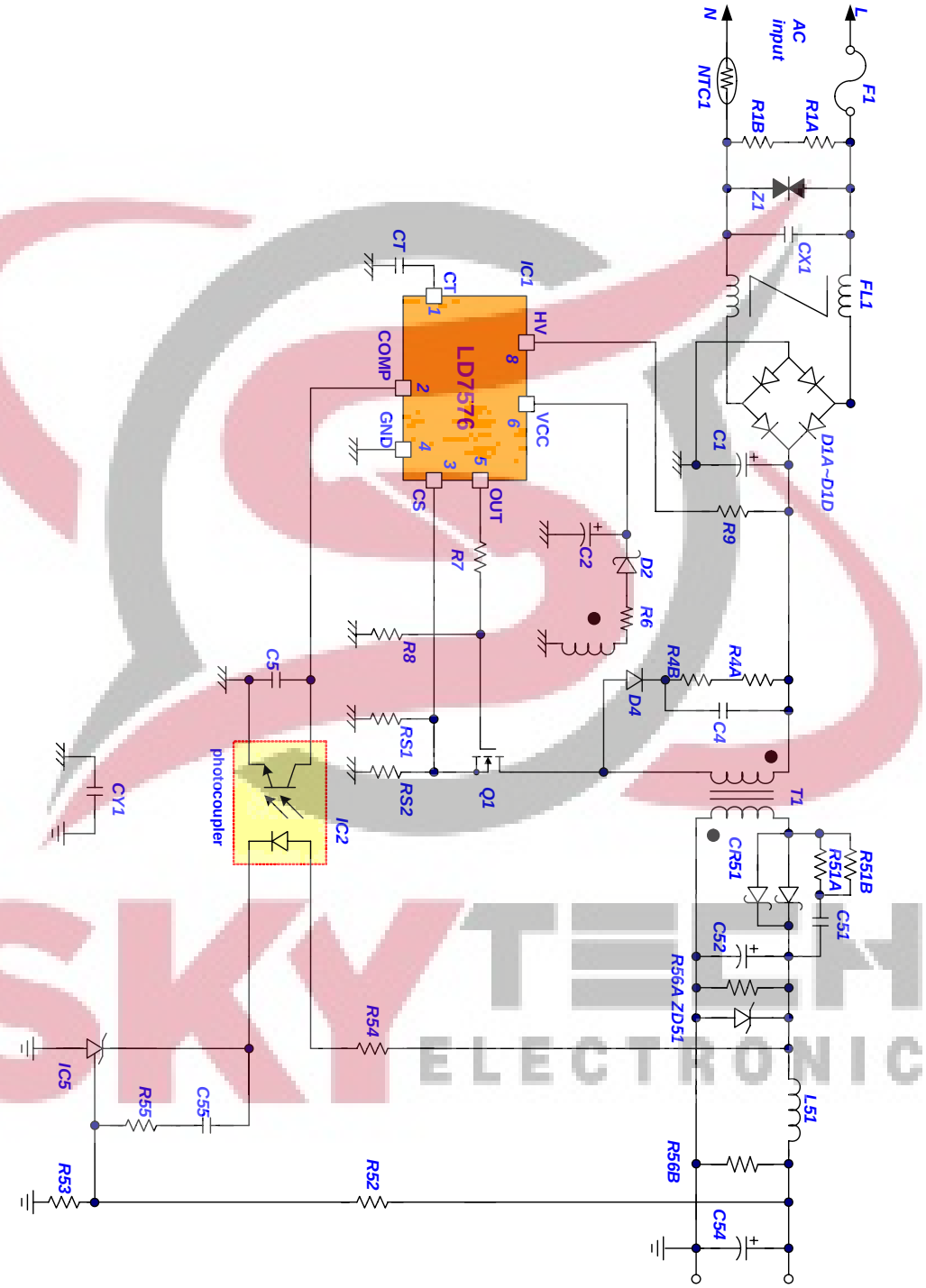


Fig. 26

Reference Application Circuit --- 10W (5V/2A) Adapter



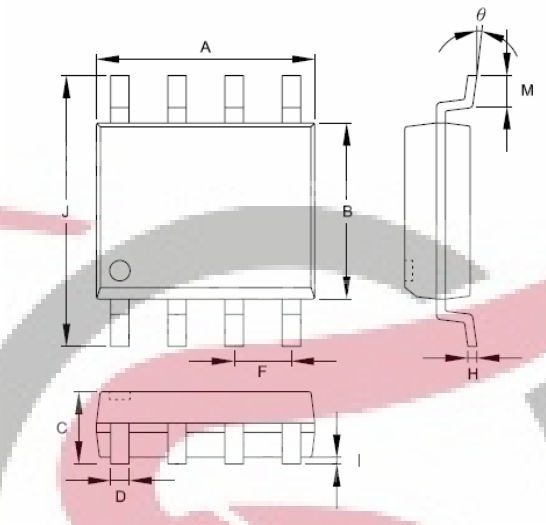
BOM

P/N	Component Value	Original
R1A	N/A	
R1B	N/A	
R4A	39KΩ, 1206	
R4B	39KΩ, 1206	
R6	2.2Ω, 1206	
R7	10Ω, 1206	
R8	10KΩ, 1206	
R9	10KΩ, 1206	
RS1	2.7Ω, 1206, 1%	
RS2	2.7Ω, 1206, 1%	
R51A	100Ω, 1206	
R51B	100Ω, 1206	
R52	2.49KΩ, 0805, 1%	
R53	2.49KΩ, 0805, 1%	
R54	100Ω, 0805	
R55	1KΩ, 0805	
R56A	2.7KΩ, 1206	
R56B	N/A	
NTC1	5Ω, 3A	08SP005
FL1	20mH	UU9.8
T1	EI-22	
L51	2.7μH	

P/N	Component Value	Note
C1	22μF, 400V	L-tec
C2	22μF, 50V	L-tec
C4	1000pF, 1000V, 1206	Holystone
C5	0.01μF, 16V, 0805	
C51	1000pF, 50V, 0805	
C52	1000μF, 10V	L-tec
C54	470μF, 10V	L-tec
C55	0.022μF, 16V, 0805	
CT	0.047μF, 10V, 0805	X5R
CX1	0.1μF	X-cap
CY1	2200pF	Y-cap
D1A	1N4007	
D1B	1N4007	
D1C	1N4007	
D1D	1N4007	
D2	PS102R	
D4	1N4007	
Q1	2N60B	600V, 2A
CR51	SB540	
ZD51	6V2C	
IC1	LD7576PS	SOP-8
IC2	EL817B	
IC51	TL431	1%
F1	250V, 1A	
Z1	N/A	

Package Information

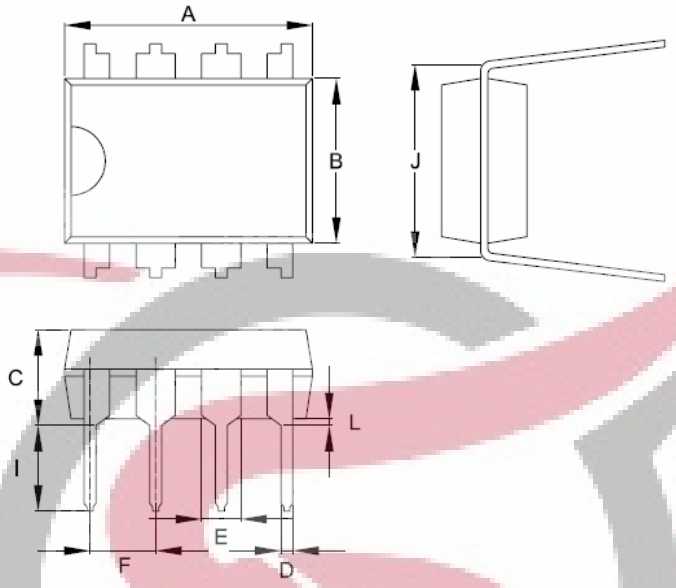
SOP-8



Symbols	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.229	0.007	0.009
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

DIP-8



Symbol	Dimension in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	9.017	10.160	0.355	0.400
B	6.096	7.112	0.240	0.280
C	-----	5.334	------	0.210
D	0.356	0.584	0.014	0.023
E	1.143	1.778	0.045	0.070
F	2.337	2.743	0.092	0.108
I	2.921	3.556	0.115	0.140
J	7.366	8.255	0.29	0.325
L	0.381	------	0.015	--------

Important Notice

Leadtrend Technology Corp. reserves the right to make changes or corrections to its products at any time without notice. Customers should verify the datasheets are current and complete before placing order.

Revision History

Rev.	Date	Change Notice
00	3/30/07	Original Specification.
01	4/23/07	Oscillator for Switching Frequency updated
02	6/21/07	Electrical Characteristics updated
03	11/30/2007	1. Features: Adjustable OLP delay time 2. Detailed Description for COMP pin capacitor. 3. Electrical Characteristics/ Low Frequency Timer 4. Green package option. 5. Block Diagram revision.